Electronic Version

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Claims

[c1] 1. A quad flat no-lead package structure, comprising:
a chip carrier having a top surface and a bottom surface, wherein a plurality of conductive leads is disposed on the bottom surface of the chip carrier, while a plurality of pads is disposed on the top surface of the chip carrier, the conductive leads being electrically connected to the pads; and
at least a chip, disposed on the top surface of the chip carrier and electrically connected to the chip carrier.

[c2] 2. The package structure as claimed in claim 1, further comprising a passivation layer to cover the chip.

[c3] 3. The package structure as claimed in claim 1, wherein the chip carrier includes an interconnect layer between the pads and the conductive leads, and wherein the interconnect layer includes at least a via for connecting one of the pads and one of the conductive leads.

[c4] 4. The package structure as claimed in claim 1, wherein the chip is electrically connected to the chip carrier through wire bonding technology.

[c5] 5. The package structure as claimed in claim 1, wherein the chip is electrically connected to the chip carrier through flip chip technology.

[c6] 6. The package structure as claimed in claim 1, wherein the chip is electrically connected to the chip carrier through surface mount technology.

[c7] 7. The package structure as claimed in claim 6, wherein an anisotropic conductive paste is further included to attach the chip and the chip carrier.

[c8] 8. A method for fabricating a quad flat no-lead package structure, comprising:
providing a substrate;
forming a plurality of metal blocks on the substrate;
forming an interconnect layer covering the metal blocks, wherein the interconnect layer includes a plurality of vias connecting to the metal blocks and a plurality of contact pads on a top surface of the interconnect layer, wherein the contact pads are electrically connected to the metal blocks through the vias;
disposing at least a chip on the interconnect layer, wherein the chip includes a plurality of bonding pads corresponding to the contact pads; and
removing the substrate to expose bottom surfaces of the metal blocks.

[c9] 9. The method as claimed in claim 8, wherein the step of forming an interconnect layer further comprises forming an oxide layer between the metal blocks and the contact pads, and wherein the vias are formed within the oxide layer for connecting the metal blocks and the contact pads.

[c10] 10. The method as claimed in claim 8, further comprising forming a passivation layer covering the chip.

[c11] 11. The method as claimed in claim 8, wherein the step of forming a plurality of metal blocks comprises the steps:
forming a metal layer on the substrate; and
patterning the metal layer to form the metal blocks.

[c12] 12. The method as claimed in claim 11, wherein the metal layer is formed by electroplating.

[c13] 13. The method as claimed in claim 11, wherein the metal layer is formed by affixture.

[c14] 14. The method as claimed in claim 11, wherein the step of forming a plurality of metal blocks further comprises forming an etching stop layer between the metal layer and the substrate, and the step of patterning the metal layer comprises:

forming a patterned photoresist layer on the metal layer;
etching the metal layer to form the metal blocks using the patterned photoresist layer as a mask; and
removing the patterned photoresist layer.

[c15] 15. The method as claimed in claim 14, wherein the step of removing the substrate further comprises removing the etching stop layer to expose the bottom surfaces of the metal blocks.

[c16] 16. A wafer-level package structure, comprising:
a wafer, having a plurality of sections;
a plurality of conductive blocks, disposed on the wafer and in each of the sections of the wafer;
a metal interconnect layer, connecting the plurality of the conductive blocks, wherein the metal interconnect layer comprises at least a via hole and a plurality of pads, wherein the via hole electrically connects one of the conductive blocks and one of the pads, and wherein the pads are disposed on an uppermost surface of the metal interconnect layer; and
at least a chip, disposed onto each of the sections of the wafer, wherein the chip includes a plurality of bonding pads that are correspondingly connected to the pads.

[c17] 17. The wafer-level package structure of claim 16, further comprising a passivation layer covering each section

of the wafer.

[c18] 18. The wafer-level package structure of claim 16, wherein the metal interconnect layer further includes an oxide layer between the conductive blocks and the pads, while the via hole through the oxide layer connects one of the conductive blocks and one of the pads.

[c19] 19. A method for manufacturing a wafer-level chip package structure, comprising:

providing a wafer having a plurality of sections;

forming a plurality of metal blocks on the wafer and in each of the sections of the wafer;

forming an interconnect layer connecting the plurality of the metal blocks, wherein the interconnect layer comprises at least a via hole and a plurality of pads, wherein the via hole electrically connects one of the metal blocks and one of the pads, and wherein the pads are disposed on an uppermost surface of the interconnect layer;

disposing at least a chip, disposed onto each of the sections of the wafer, wherein the chip includes a plurality of bonding pads that are correspondingly connected to the pads; and

removing the wafer to expose bottom surfaces of the metal blocks.

[c20] 20. The method of claim 19, wherein the step of forming

an interconnect layer comprises forming at least an oxide layer between the pads and the metal blocks, and wherein the via hole through the oxide layer electrically connects one of the metal blocks and one of the pads.

[c21] 21.The method of claim 19, further comprising forming a passivation layer covering each section of the wafer.

[c22] 22. The method of claim 19, wherein the step for forming the metal blocks comprises forming a metal layer over the wafer and then patterning the metal layer to form the metal blocks on the wafer.

[c23] 23. The method of claim 22, wherein the metal layer is formed by electroplating.

[c24] 24. The method of claim 22, wherein the metal layer is formed by coating or affixture.

[c25] 25. The method of claim 22, wherein step of patterning the metal layer comprises:

forming an etching stop layer on each section of the wafer;

forming a patterned photoresist layer on the metal layer;

performing etching to define the metal blocks; and

removing the patterned photoresist layer.

[c26] 26. The method of claim 25, wherein the step of remov-

ing the wafer further includes removing the etching stop layer to expose the bottom surfaces of the metal blocks.